Appln. No.: 10/700,275
Amdt. dated 11/17/05

Amendments to the Claims:

Please amend claims 44-48 and 50-54, and cancel claim 49 as shown in the following listing of claims. This listing of claims will replace all prior versions and listings of claims in the application:

1-42. (cancelled)

43. (previously presented) A method for generating a set of clock signals in a system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of input signals and a receive clock signal, the system comprising a set of subsystems, each of the subsystems comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, each of the subsystems comprising a digital section, each of the digital sections operating in accordance with the receive clock signal, the method comprising the operations of:

(a) receiving a plurality of transmitted signals;

(b) generating phase control signals associated with each of the plurality of transmitted signals;

(c) generating a receive phase control signal for the receive clock signal in accordance with at least one of the phase control signals;

(d) generating the sampling clock signals in accordance with the corresponding phase control signals; and

(e) generating the receive clock signal in accordance with the receive phase control signal.

44. (currently amended) The ~~timing recovery system~~ method of claim 43 wherein the receive clock signal is related to one of the sampling clock signals.

45. (currently amended) The ~~timing recovery system~~ method of claim 44, wherein generating step (c) comprises adding one of the phase control signals to a receive clock offset to generate a phase shift value ~~further comprising a first adder and a receive clock phase selector, the first~~

~~adder receiving one of the phase control signals and a receive clock offset and generating a phase shift value, the receive clock phase selector receiving the phase shift value and generating the receive clock signal~~.

46. (currently amended) The ~~timing recovery system~~ method of claim 45 wherein the phase shift value comprises a set of phase steps and wherein ~~the receive clock phase selector receives~~ generating step (e) comprises receiving the phase shift value in the form of consecutive phase steps.

47. (currently amended) The ~~timing recovery system~~ method of claim [[41]] 43 wherein the set of clock signals further comprises a transmit clock signal and wherein each of the subsystems further comprises a transmit section, the transmit sections operating in accordance with the transmit clock signal.

48. (currently amended) The ~~timing recovery system~~ method of claim 47 further comprising ~~a transmit clock phase selector, the transmit clock phase selector~~ receiving a transmit clock offset and generating the transmit clock signal in accordance with the transmit clock signal.

49. (cancelled)

50. (currently amended) The ~~timing recovery system~~ method of claim 47 wherein the transmit clock signal is related to one of the sampling clock signals.

51. (currently amended) The ~~timing recovery system~~ method of claim 50 further comprising a ~~transmit clock phase selector, the transmit clock phase selector~~ receiving one of the phase control signals and generating the transmit clock signal in accordance with the phase control signal.

52. (currently amended) A timing recovery system for generating a set of clock signals in a processing system, the set of clock signals comprising a set of sampling clock signals associated with a corresponding plurality of ~~input~~ transmitted signals and a receive clock signal, the processing system comprising a set of processing subsystems, each of the processing subsystems

comprising an analog section, each of the analog sections operating in accordance with a corresponding one of the sampling clock signals, each of the processing subsystems comprising a digital section, each of the digital sections operating in accordance with the receive clock signal, the timing recovery system comprising:

(a) a decoder for generating a plurality of signals associated with the plurality of transmitted signals; and

(b) a timing recovery circuit for receiving the signals generated by the decoder, and for generating phase control signals associated with each of the plurality of transmitted signals and a receive phase control signal for the receive clock signal in accordance with at least one of the phase control signals, wherein the timing recovery circuit generates the sampling clock signals in accordance with the corresponding phase control signals and generates the receive clock signal in accordance with the receive phase control signal.

53. (currently amended) The timing recovery system of claim [[41]] 52 wherein the set of clock signals further comprises a receive clock signal and wherein each of the processing subsystems further comprises a digital section, the digital sections operating in accordance with the receive clock signal.

54. (currently amended) The timing recovery system of claim [[41]] 52 wherein the set of clock signals further comprises a transmit clock signal and wherein each of the subsystems further comprises a transmit section, the transmit sections operating in accordance with the transmit clock signal.